IN THE SPECIFICATION:

Please amend the specification on page 5, lines 19-21 as follows:

--Figure 2 is a block diagram illustrating the novel clock signal adjustment circuit implementing ~~implementing~~ data error checking according to a second embodiment of the invention.--

Please amend the specification from page 6, line 7 through page 7, line 2 as follows:

--Figure 1 is a block diagram depicting the novel error correcting system architecture 10 according to a first embodiment of the invention. As shown in Figure 1, there is provided a source circuit device 12 for transmitting data signals through ECC error correction circuitry 20 to a destination device such as IC receiver device 15 according to clock timing signals 18 provided by clock generator circuit 30. As shown in Figure 1, the source transmitter circuit 12 is coupled to an error correcting code (ECC) generator circuit device 20 that generates ECC bits in accordance with the data that is received from the transmitter 12. The ECC generator 20 receives data from the transmitter 12 and, outputs the data plus error correction information according to known techniques. Coupled to the ECC generator device 20 is a novel error correcting code (ECC) check circuit device 25 which, in turn, is coupled to a destination receiver device 15 for receiving the transmitted data. As will be described in further detail herein, ECC generate 20 and ECC check 25 devices ensure the integrity of real data 19 communicated between respective transmit source and destination receive circuits 12, 15 within the IC. As shown in Figure 1, the system architecture 10 is provided with an input reset signal ~~28~~ 27 which when activated, triggers a system learning cycle for initializing clock timing signals so that data transmission rates may be optimized according to the characteristics of the IC. –

Please amend the specification from page 7, line 18 through page 8, line 9 as follows:

--Figure 2 is a block diagram depicting the novel error correcting system architecture ~~30~~ 29 according to a second embodiment of the invention. As shown in Figure 2, the transmitter, receiver and clock generator circuits are identical to the like elements depicted in Figure 1, however, there is included a novel error check ~~error check~~ circuit 33 that checks for errors in real time. At reset, a learning cycle is implemented where a series of predefined error code transmissions or, a pseudo random bit streams, are generated from the transmit source 12 destined for error check circuit 33 over error codes lines 55. It is understood that the error code lines may comprise a single conductor or even a data bus. In accordance with this second embodiment, implementing wiring tools during the final production development phase, i.e., "PD" cycles, the load on the error codes lines 55 is fixed in such a way to provide a signal delay, as compared to data traveling over data line 19 directly from the transmitter 12 to the receiver 15. In one embodiment, the delay may be accomplished with capacitive loading, for instance of conductors 55.--

Please amend the specification from page 8, line 11 through page 9, line 14 as follows:

-- Preferably, according to the second embodiment, at reset, a learning cycle is implemented where a series of predefined transmissions is generated from the transmit source 12. According to the invention, during the test time, the error check circuitry 33 (Figure 2) will monitor to a first fail point, and then pick a clock tap of sufficient guard band to guarantee the error free arrival of the data. That is, as the error check circuit ~~30~~ 33 is informed of the bit signal patterns output from the transmitter, it knows what signals to expect at each iteration. Thus, during the learning cycle, for each one

or a series of outputs generated from the transmit source 12, the clock signal 18 is gradually increased, for example. Thus, the generated signal patterns along line 55 are sufficiently delayed so that they may be read by the error checker circuit 33. As the clock signal 18 input to the transmitter effects the timing of signals generated at the transmit source 12, the error check circuit will monitor the delayed transmitter output, and verify whether the correct data signal patterns were correctly received. As soon as a failure is detected or a failure rate that exceeds a minimum threshold is detected at the error check circuit 33, indicating an excessive clock speed 18, a signal 32 may be fed back to the clock generator circuit 30 in order to decrease the clock speed. The clock speed may be adjusted until no failures are detected at the error check circuit, or at least until failures are detected below a certain failure rate. It should be understood that, in order to insure that the error correction wires are slower than the rest of the bus, the wiring tool may introduce deliberate delay though the use of additional delay buffers and capacitance on the wires forming the error correction lines 55 which would cause the error bits to be the first to fail. The data path would still be intact and allow the data to still be transmitted while the clock generation circuit is being slowed down. In order to implement this setup, the error correction code requires it's own error correction to be able to identify that the ECC signals were the ones that were failing.--

Please amend the specification from page 11, line 10 through page 12, line 6 as follows:

--Particularly, this random data 56 is fed to the start of the dataflow path 56a at the input of the CORE circuit 60 and the data is transmitted through various asynchronous busses or serial data streams. In one embodiment depicted in Figure 3, processing flow through the CORE circuit 60 includes devices such as data busses 57a, 57b and various logic block/bridges 58a, 58b to the output. Finally, the random data arrives at a data bus output 57b as data output signal 65, and is returned back to the comparator

device 70 provided in the optimizer 39. In the optimizer 39, the original random data 56 is input to the error detecting comparator device 70 implementing logic for comparing the random data 65 received from the CORE 60 to the random data 56 that was sent into the core 60. If the data is correct, the output of the comparator circuit 70 will generate signals ~~32~~ 80 for enabling the clock frequency provided by clock generator circuit 30 to be increased. That is, if the system on chip (SOC) is operating at an operable frequency and no data errors occur, then the data 65 received will match the data 56 that what was sent and the clock frequency may be increased. If the data does not match, then the system clock 30 is running too fast and the frequency must be decreased. That is, if any errors are found as a result of the comparison, the clock taps 34 provided in clock generator circuit 30 may be increased to step down the clock frequency. Thus, as shown in Figure 3, the frequency of clock signal 30 is chosen from several clock taps via a multiplexor 72.--